Current harmonics compensation for electrolytic processes using a series active scheme

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Abstract: A series active filter to compensate current harmonics injected by high-power rectifiers [such as in copper electro-winning (EW) and electro-refining (ER) processes] is presented and analysed. The proposed current harmonic compensation method is accomplished by injecting a corresponding series voltage distortion at the rectifier ac terminals. The distorted ac voltage generated at the high-power rectifier ac terminal forces the line current to be sinusoidal and increases dc voltage distortion, but it does not affect the EW or ER processes. A complete design procedure for the series active system is presented. In conjunction with simulated results obtained from a 10 MVA copper EW facility, a 2 kVA laboratory prototype is used to validate the current harmonic compensator scheme. The results obtained through simulation and from the experimental prototype confirm the viability of the proposed compensator and associated control strategy.

1 Introduction

Copper electro-winning (EW) and electro-refining (ER) processes use high-current rectifiers to treat processed copper solutions. Commonly, a multi-pulse arrangement of paralleled six-pulse thyristor phase-controlled rectifiers is used. Phase-controlled rectifiers introduce current distortion into the system and present a lagging power factor. The arrangement of multi-pulse converters and passive filters must be designed in order to obtain unity power factor operation and effectively lower current distortion to a level consistent with IEEE Standard 519, even if one of the six-pulse rectifiers fails. Passive filters composed of different branches must distribute the required reactive power generated by each branch. In general, passive filters include dedicated low-order harmonic filters with reactive power compensation capacity, even when multi-pulse arrangements of step-down transformers are used [1–3]. These filters are also used to avoid low-frequency resonances, which can cause magnetic saturation in the step-down transformer core. For example, a typical 10 MVA EW plant requires the on-site installation of a 5.0 MVAR filter with branches tuned at 5, 7, 11 and 13 (see Fig. 1a). This compensation scheme presents a number of drawbacks, such as high-rating power of passive filter components, possibility of power distribution system resonances and requisite large physical space to install the filters (5000 ft\(^3\)) [4].

Alternative pulse-width-modulated (PWM) rectifier configurations aimed at improving the electrical performance of long-used thyristor-based configurations have been reported in the literature [4, 5]. An extensive evaluation of the operation, configuration and electric properties of thyristor and PWM rectifiers is presented in [6], concluding that in the future PWM rectifiers will become a very attractive alternative to replace thyristor rectifiers. PWM rectifiers eliminate the need for reactive power and low-frequency current harmonic compensation by pushing harmonic current compensation to higher frequencies. However, because this trend is conditioned by the development of high-voltage reverse-blocking semiconductors, it is not yet possible to apply PWM rectifiers to high-power rectifiers. At the same time, interest in active power filter (APF) applications has increased considerably owing to concerns of power quality impact [7]. Shunt, series and hybrid active filters have been presented as a flexible integration technology for 1–10 MVA power range industrial applications [8, 9]. APFs have the potential for attenuating supplied current harmonics and compensating reactive power [1, 10–13]. Although custom power devices have been available for over a decade, the market has been reluctant to adopt the technology because of its high cost and inadequate reliability and availability levels, which have yet to meet utility expectations.

Typically, series active filter connection is used to compensate voltage distortion, sags, swells and imbalance, whereas shunt active filter connection is used for current harmonic distortion and load power factor compensation [14–16]. Another topology is the hybrid filter [17, 18], which employs a combination of an active series filter and a passive filter, and is becoming an interesting alternative for medium voltage applications. Series active filters that have been used only to compensate voltage regulation, sags, swells and imbalance are known as dynamic voltage restore (DVR). Such equipment is not designed for and has not been used to compensate current harmonic. However, series APFs in combination with passive filters connected in
parallel have proved to be a good solution for current harmonic compensation [17]. In this scheme, the series active filter operates as a variable voltage source at the frequencies in which current harmonics need to be attenuated. Compared with well known shunt APF schemes, the proposed series active topology is more suitable for compensation of phase-controlled high-power rectifiers because of the requirements of smaller-rated power filter converter values and good current harmonics compensation performance. Moreover, voltage regulation capabilities can be implemented by a simple modification in the control scheme, so it can behave as a DVR as well as current harmonic compensator. In terms of losses and efficiency, the proposed scheme shows better performance than traditional passive filter schemes. Passive filters used to compensate reactive power and current harmonics are normally C-type high-pass, with a resistance in parallel with the inductor. Depending on the filter-rated power, losses in each filter can reach several hundred kW [1]. Since the proposed APF is implemented with a PWM voltage-source inverter (VSI), losses are below 5% of the converter-rated power.

This paper proposes a series active filter scheme for EW and ER high-current rectifiers [19]. The proposed compensator is designed to operate as a harmonic isolator, eliminating the need for passive tuned filters. These characteristics are achieved by injecting a distorted voltage at the rectifier ac terminals. Consequently, the rectifier operates with a distorted input voltage, which introduces voltage distortion at the low dc (direct current) voltage (few hundred volts) and high-current (in the order of kilo Amps) electrolytic cells load. Therefore the output voltage \( V_o \) is composed of a controllable dc average component and low-frequency voltage harmonic components. In electrolytic cells, ripple voltage in the dc bus does not affect the metallurgical process. The amount of dc current cells is regulated by the difference between the reaction voltage \( V_{ce} \) and the dc average output rectifier voltage. The average design output rectifier dc voltage must be slightly higher than the cells’ voltage. For this reason, a dc load voltage distortion does not affect the operation of the electrolytic process.

This paper presents a complete analysis of the proposed series active filter, including principles of operation, control system and filter design as key points of analysis. Simulated results obtained using a real 10 MVA rectifier facility prove the compensation effectiveness of the proposed series active scheme. Experimental input current and voltage waveforms obtained from a 2 kVA prototype prove the compensation effectiveness and technical viability of the proposed scheme.

2 Compensator topology and operating principles

Fig. 1b shows the proposed series APF topology composed of three identical single-phase PWM VSIs with LC high-frequency output filters. To take advantage of the single-phase PWM inverter implementation, the APF allows for series connection of more than one single-phase unit, instead of three-phase converter implementation, as shown by the dotted line in Fig. 1b. The APF implemented with single-phase PWM inverters connected in cascade presents key advantages in terms of compensation flexibility (e.g. unbalanced currents and control simplicity). Moreover, cascade connection of single-phase units allows the cancellation of harmonics components associated with the inverter PWM switching technique [20]. Each VSI shares the same dc-bus voltage \( V_c \), avoiding problems associated with independent dc-link control and each reduces the number of control loops [21]. A reduced number of control loops represent a significant simplification in the design and
operation of the APF. Another important characteristic of single-phase PWM inverters is that dc voltage frequency components are associated with the inverter switching frequency; therefore no second harmonic exists.

The VSI’s are connected in series to the power distribution system through coupling transformers. In Fig. 2, \(v_{SAF}\) represents the voltage waveform injected by the series APF, \(v_L\) the voltage at the system equivalent series inductance, \((v_s - v_L)\) the point of common coupling (PCC) voltage, and \(v_R\) the voltage at the high-power rectifier ac terminals. In order to attenuate line-current harmonics, the series APF presents a high equivalent impedance to harmonic currents, thus acting as a voltage source to block harmonic current flow. As a result, the rectifier voltage waveform at the rectifier terminals is modified and the system current \(i_s\) is forced to be more sinusoidal. The equivalent circuit shown in Fig. 3 explains the principles of operation of the fundamental and harmonics frequency components. Referring to Fig. 3, if \(G \gg jkX_s\), then the system current harmonic is given by (1)

\[
i_{hk} = \frac{(v_{PCC} - v_{R})}{jkX_s + G} \approx \frac{(v_{PCC} - v_{R})}{G}
\]

If the gain \(G\) is high enough (at least 10 times larger than \(kX_s\)), \(jkX_s\) can be neglected and the line current harmonic component can be attenuated significantly. In this case, the APF equivalent impedance behaves as a current controlled harmonic voltage source \(G_{i_{hk}}\) (2). Therefore near-sinusoidal three-phase currents are drawn from the utility.

\[
v_{SAF} = G_{i_{hk}} + v_{SAF1}
\]

One of the advantages of active filtering is that reactive power compensation and current harmonic can be achieved simultaneously. However, current harmonic and reactive power compensation can also be decoupled and controlled independently. The proposed APF can perform both compensations simultaneously or sequentially, depending on the control structure. If both compensations are required, the converter’s apparent power must be increased. If reactive power compensation is required, the magnitude of the fundamental voltage component of the injected voltage is controlled by keeping the PCC voltage in phase with the system current, allowing unity power factor. In this approach, reactive power compensation is determined with the phasor diagram shown in Fig. 4, where \(\phi_1\) is the phase angle between the load voltage and the system current, and \(v_{SAF} - Q\) must be generated by the APF to compensate the utility power factor. The amplitude of the \(v_{SAF} - Q\) fundamental component must satisfy (3)

\[
v_{SAF} - Q \geq 2v_s \sin\left(\frac{\phi_1}{2}\right)
\]

If the proposed series APF is used to compensate only current harmonics, the voltage at fundamental frequency injected by the PWM converter must present a small amplitude, which is adjusted by the small amount of active power absorbed by the converter. In order to fulfill current harmonic compensation effectiveness, the series active filter must be able to generate a voltage \(v^*_{SAF}\), whose amplitude is calculated through the control scheme shown in Fig. 5.

3 Control system

Fig. 5 shows the proposed control system block diagram. It comprises a dc voltage control loop, a reference signal generator, which provides the current reference waveform \(G_{i_{hk}}\) and a gating signal generator.

3.1 Reference signal generator

Each line current is introduced into a phase-locked-loop (PLL) block (Fig. 6). A single-phase PLL structure implemented with a second-order generalised integrator (SOGI) [22] is used to extract the fundamental component of the system line current (Fig. 6). This fundamental component extraction method has the advantages of fast and accurate signal-tracking capabilities, few hardware components (since it requires 50% of multipliers compared with the synchronous reference frame PLL method [23]).
Replacing $s$ with the discrete transfer function of the second-order integrator (5) in (4), a discrete form of the closed-loop transfer function is obtained (6)

$$
H(z) = \frac{c_1 z^{-1} - c_2 z^{-2} + c_3 z^{-3} + c_4 z^{-4}}{2(1 - z^{-1})}
$$

where, $c_1 = (3/2)k_c \omega T_s$, $c_2 = -4(3/4)c_1$, $c_3 = c_1/3$, $c_4 = 2 - c_1$, $c_5 = -1 - c_2 + 9c_7$, $c_6 = -c_3 - (8/3)c_7$ and $c_7 = -(1/4)k_c \omega T_s$. For a sample frequency of 6103 Hz and $k_c = 1$, the following constants are used: $c_1 = 0.0771$, $c_2 = 0.1029$, $c_3 = 0.0256$, $c_4 = 1.9227$, $c_5 = 0.9031$, $c_6 = 0.0217$ and $c_7 = 0.0006$.

The signal flow graph shown in Fig. 6 shows how to implement a SOGI-PLL in a discrete form (6), as required for FPGA implementation. The subscript $k$–$M$ represents the time delay associated with $M$ samples per cycle. Since the execution time is equal to 1 $\mu$s and is not higher than the sample frequency, SOGI-PLL is a good solution to obtain the fundamental current waveforms without time delay.

Finally, the system line currents and the extracted fundamental currents in each phase are subtracted to obtain the current harmonic components that need to be compensated. The current harmonic components are amplified with a well-defined control gain $G$, and the result is applied to the gating signal generator as part of the voltage reference $v_{SAF}$. The gain $G$ depends on the APF compensation effectiveness and its value has an impact on the APF’s rated power, as demonstrated in Section 4.3.

### 3.2 Gating signal generator

A triangular waveform synchronised with system voltage is generated. This triangular waveform fixes the semiconductor switching frequency. There are two important variables to consider when specifying the switching frequency in high-power APFs. Higher switching frequency is required to filter higher harmonics; however, the semiconductor power capacity limits the switching frequency. In this case, a 1.5 kHz switching frequency is selected to emulate high-power commercially available PWM converters. Then, a three-phase synchronous reference frame PLL is used to generate a sawtooth waveform ($oa$) in phase with $v_a^o$. The synchronised sawtooth waveform is used to read a triangular waveform (tri) stored in the 4096 x 12-bit internal FPGA ROM memory. The triangular waveform accuracy is limited by the maximum number of periods that produces a minimum of $n$ triangular points per cycle. In this case, $n$ is 18 and the triangular waveform frequency is 1.5 kHz. Then, the gating signal generator produces unipolar fixed frequency switching signals for each single-phase inverter by comparing $v_{SAF}$ and triangular, as shown in Fig. 8.

### 3.3 Dc-voltage control

The dc capacitor remains constant until the active power absorbed by each inverter decreases to a level that is not able to supply its losses. The active power absorbed by each inverter is controlled by adjusting the amplitude of the fundamental component voltage ($v_{SAF}$), which is in phase.
with each line current. Since the three inverters share the same dc capacitor, only one PI control is required, as shown in Fig. 9. The parameter used is the inverter dc-bus voltage \( V_C \), which is controlled through the active power balance requirement.

In the block diagram shown in Fig. 9, the dc capacitor voltage \( V_C \) is measured using a voltage transducer \( K_{sv} \) and then is compared with the reference value \( V_C^* \). The error is processed by a PI controller, with two gains: \( K_p \) and \( T_i \); both gains can be calculated according to the dynamic response requirement. The output of the PI control is fed to each VSI power block \( G(s) \), which is represented as a first-order system (7).

\[
G(s) = \frac{\Delta V_C}{\Delta V_C^*} = \frac{3 \sqrt{2} \cdot K \cdot i_s \cdot \cos(\phi)}{2 \cdot s \cdot C_{DC} \cdot V_C^*} \tag{7}
\]

A sinusoidal signal, extracted by the reference signal generator circuit, is added to the proportional harmonic current waveforms. The amplitude of the sinusoidal signal is modified by the PI controller. The closed-loop transfer function of the given system with a PI controller (8) is shown below (9)

\[
C(s) = K_p \left(1 + \frac{1}{s T_i} \right) \tag{8}
\]

\[
\frac{\Delta V_C}{\Delta V_C^*} = \frac{a^2_0 \cdot a \cdot (s + a)}{s^2 + 2 \zeta \omega_n \cdot s + \omega_n^2} \tag{9}
\]

By adding the sinusoidal signal to the input of the gating signal generator, the active power flowing into the capacitor will change, controlling the dc capacitor voltage.

The time response of the dc voltage control loop does not need to be fast because of the slow dynamics of the electrolytic capacitor. The proportional and integral (PI) gains must be tuned for a critically damped response. In this case, damping factor \( \zeta = 1 \) and natural angular speed \( \omega_n = 2 \pi \cdot 100 \text{ rad/s} \) are used. The corresponding integral time \( T_i = \frac{1}{a} \) (9) and proportional gain \( K_p \) can be calculated from (10) and (11).

\[
T_i = \frac{4}{3} \frac{\sqrt{2} \cdot C_{dc} \cdot V_C^*}{K_p \cdot i_s \cdot \cos(\phi)} \tag{10}
\]

\[
K_p = \frac{2 \zeta \omega_n \sqrt{2} \cdot C_{dc} \cdot V_C^*}{3K_p \cdot i_s \cdot \cos(\phi)} \tag{11}
\]

### 4 Active power filter design

#### 4.1 Dc capacitor

The dc capacitor value is obtained by using (12). With this value, the capacitor is able to store enough energy to supply the instantaneous power required by the ac system during half a cycle, without changing the dc voltage value by more than 5%.

\[
C_{dc} \geq \frac{T}{2} \frac{v_{sm}i_{sm}}{V_C^2 - V_C^*} \tag{12}
\]

where \( v_{sm} \) is the ac system phase to neutral voltage peak value, \( i_{sm} \) is the root mean square (rms)-rated load current, \( T \) is the ac system period, \( V_C \) is the dc voltage reference value and \( V_C^* \) is the minimum voltage allowed at the dc bus.

#### 4.2 LC output filter

The second-order LC filter connected at the inverter ac terminals eliminates the ripple voltage generated by each single phase PWM full bridge inverter. Its design is based on the maximum voltage harmonic ripple allowed at the coupling transformer terminals and with unity filter gain at the fundamental frequency. The filter must not attenuate the low-frequency voltage harmonics required to compensate the load current harmonic.

From Fig. 10, in order to calculate \( L_f \) and \( C_f \), the system equivalent impedance at the switching converter frequency, \( Z_{sys} \), reflected at the secondary winding must be known and can be represented as

\[
Z_{sys(secondary)} = (n_2/n_1)^2 Z_{sys(primary)} \tag{13}
\]

At the switching frequency, the following design criteria must be satisfied:

1. \( X_C \ll X_{L_f} \), to ensure that at the switching frequency most of the inverter output voltage will drop across \( L_f \).
2. \( X_C \) and \( X_{L_f} \ll Z_{sys} \), to ensure that the voltage divider is between \( L_f \) and \( C_f \).

In this example, \( L_f = 9.3 \text{ mH} \) and \( C_f = 3.6 \mu \text{F} \) are obtained considering a series transformer with a turn ratio of 1:1 to ensure galvanic isolation, assuming \( X_{L_f} = 10X_C \) and \( L_s = 2\% \), with reference to base values of \( V_{base} = 13.8 \text{kV} \).
and $S_{\text{base}} = 10 \text{ MVA}$. The selected transformer’s turn ratio limits the insulated gate bipolar transistors (IGBT’s) current to commercially available IGBT modules that are able to block high-voltage levels of $6.5 \text{ kV}$ (ABB – 5SNA 0750G650300). To operate IGBTs at lower voltage, the series transformer turn ratio must be increased, but the secondary current will also increase. The best combination between voltage and capacity of current semiconductors must be selected.

4.3 Rated apparent power

Since APFs can be used for reactive power as well as current harmonic compensation, the required apparent power of the converter changes. In order to compensate for reactive power, the rms voltage required at the inverter output terminals is higher, and can be obtained by using (3). If the APF is used to compensate only current harmonics, a small rms voltage is required at the inverter’s ac terminals. The rated compensating voltage of the APF is equal to the rms value of the harmonic components. The harmonic components are calculated considering typical 12-pulse line currents drawn from the three phase lines. According to (2), the APF must generate $12p + 1$-th harmonic voltage components. Therefore the rated compensating voltage is calculated as

$$v_{\text{SAF}} = \sqrt{\sum_{n=1}^{N} \left( \frac{G_n}{12n} \pm 1 \right)^2 + v_{\text{SAF}}^2}$$  \hspace{1cm} (14)$$

where $G$ is the compensating control gain, $i_s$ is the rms line system current and $v_{\text{SAF}}$ is the fundamental voltage component that provides the active power required to supply inverter losses. The required VA rating of the APF is given by (15), and is composed of two parts. One represents a constant line voltage draw and the other represents a variable compensation voltage.

$$S_{\text{SAF}} = \sqrt{3}v_{\text{SAF}}i_s$$  \hspace{1cm} (15)$$

Equations (14) and (15) demonstrate that the compensator’s rated power depends on the compensation functions, since they define the magnitude of the injected voltage. Considering that a typical phase-controlled rectifier operates with a phase-shift angle equal to 30° in EW or ER applications, the reactive power that needs to be compensated can be calculated, as can the amplitude of the current harmonics that need to be eliminated. Therefore if the APF aims to perform both compensations, the required apparent power goes up to 40% of the 10 MVA compensated non-linear load. However, if only current harmonics are compensated, the amplitude of the required voltage is reduced, and therefore the required apparent power of the static converter reduces to only 20% of the 10 MVA non-linear load.

5 Active power filter compensation performance

5.1 Simulation

In order to prove the compensation effectiveness of the proposed scheme, a 10-MVA copper EW system was simulated, with the following dc parameters $R_{\text{dc}} = 0.3 \Omega$, $L_{\text{dc}} = 5 \text{ mH}$ and $V_{\text{dc}} = 200 \text{ V}$. The Series AF was tested compensating a 12-pulse high-current rectifier. Simulations were performed using PSIM software. Table 1 shows the parameter values of the proposed LC filter in p.u. and its respective absolute values, with reference to 10 MVA and 13.8 kV base values. The control gain $G$ of the active filter is set at 10 pu, which is equal to 190 $\Omega$. The rated kVA of the series active filter is 36% (360 kVA) of the load rated power. In this case, the series APF compensates for current harmonics and reactive power.

Figs. 11 and 12 show simulated waveforms before and after the series active filter starts compensation. Before connecting the active filter, the total harmonic distortion (THD) of $i_s$ is 9.58%, as shown in Fig. 11a. By compensating with the series APF, the line current THD is reduced from 9.58 to

| Table 1 | LC passive filter values ($V_{\text{base}} = 13.8 \text{ kV}$ and $S_{\text{base}} = 10 \text{ MVA}$) |
|------------------|---------------------|---------------------|
| $L_f$            | 9.3 mH              | 0.154               |
| $C_f$            | 3.6 $\mu$F          | 0.022               |
| $C_{\text{dc}}$ | 3300 $\mu$F         | 5.98                |

Fig. 11 Simulated waveforms

- a System voltage and rectifier input current after compensation
- b System voltage and current with the proposed SAF ($V_{\text{base}} = 13.8 \text{ kV}$ and $S_{\text{base}} = 10 \text{ MVA}$)
- c Log comparison between supply current harmonic spectrum expressed as the harmonic-to-fundamental current ratio. (For $i_s$, THD = 9.58% and for $i_s(SAF)$, THD = 3.55%)
3.55%, as shown in Fig. 11b. Moreover, load power factor is also improved from 0.94 before compensation up to 0.98. For harmonic components, the series APF behaves as an equivalent 190 V resistor. A comparison in logarithmic scale of the two-frequency spectrums is plotted in Fig. 11c, and shows the harmonics reduction using the proposed series APF. Fig. 12 demonstrates that even though the rectifier dc voltage is distorted with a ripple factor equal to 5.97%, owing to the effect of the series APF, the dc current remains constant, with almost zero ripple.

5.2 Experimental waveforms

In order to validate the proposed active compensation scheme, a 2 kVA laboratory prototype using IGBT switches was implemented. Each inverter was operated at 1.5 kHz switching frequency. This small switching frequency emulates the proposed scheme in the high-power range. The transformer’s turn ratio is 1:3. The active filter dc-bus capacitor is 2700 μF. The control strategy, modulation and
Fig. 15 Experimental results

Series AF VSI output voltage and capacitor voltage after starting SAF, \( CH1 = V_{SAF} \) and \( CH2 = V_C \)
synchronisation with the grid were implemented on an FPGA Nexys 2 Board from Digilent Inc. For the sake of simplicity, an \( R-L \) load type was connected at the rectifier dc bus instead of an \( R-L-V \). The rectifier dc load was implemented with a 6 mH inductance and an adjustable resistor. The rectifier was connected to a 380 V, 50 Hz power supply. Fig. 13 shows the reference signal generator waveforms. Fig. 13 also shows the load current fundamental component \( i_1 \), obtained from the SOGI filter, and synchronous reference frame (SRF)-PLL output waveform, \( s(t) \), which is synchronised with the system phase-voltage \( v_s(t) \).

Experimental steady-state results demonstrate the feasibility of the proposed compensation scheme performance and validate the effectiveness of the control strategy implemented. Figs. 14a and b show the input system currents before and after starting active series compensation. The input system current waveform shown in Fig. 14b is as expected. As shown in the simulated results, the system current becomes more sinusoidal and the THD is reduced from 10.10 to 4.90%. The same frequency spectrum comparison used in the simulation results is plotted in Fig. 14c and shows the current harmonic components’ reduction using the proposed series APF.

The voltage at the output of each VSI (Fig. 15) has the fundamental component required to supply the losses in the inverter and in the coupling transformers. In order to obtain a better compensation performance response, a coupling transformer implemented with ferrite core was used instead of a typical silicon steel core transformer.

6 Conclusions

A series APF that is able to compensate current harmonics injected by high-power rectifiers was proposed in this paper. The series APF circuit scheme is characterised by the integration of small-rated single-phase PWM-VSI units connected in series, sharing the same dc-bus. Experimental results obtained in a 2-kVA laboratory system demonstrated the feasibility and effectiveness of the proposed series APF.

Current harmonic compensation was achieved by distorting the voltage at the rectifiers ac terminals. Therefore the proposed current harmonic compensation scheme does not require passive filters. Power circuit design and control scheme design procedures for the proposed series APF were reported in the paper.

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8 References


